Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) The integrated circuit according to claim 16, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck).

3. (Previously Presented) The integrated circuit according to claim 2, wherein the transistor threshold voltage is determined by a bulk voltage of at least one transistor in a computational island.

4. (Previously Presented) The integrated circuit according to claim 16, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, or clock frequency value.

5. (Previously Presented) The integrated circuit according to claim 16, wherein the pre-set level of performance relates to at least one of power consumption or speed of the integrated circuit.

6. (Previously Presented) The integrated circuit according to claim 16, wherein each computation island is located in an isolated third well of a triple-well CMOS technology.

7. (Cancelled)

8. (Currently Amended) The integrated circuit according to claim [[7]] 16, wherein at least two interface islands are located in a common third well, or a substrate, of a triple-well CMOS technology.

9. (Previously Presented) The integrated circuit according to claim 16, wherein each of the first and second computation islands further comprises an actuator for tuning the at least one utility value in a monitored utility value-regulating closed-loop system.

10. (Previously Presented) The integrated circuit according to claim 16, wherein each of the first and second computation islands further comprises a local monitor for monitoring local working parameters.

11. (Cancelled)

12. (Previously Presented) The method according to claim 17, wherein the at least one utility value comprises one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck).

13. (Currently Amended) The method according to claim 17, wherein the at least one working parameter further comprises at least one of ~~circuit activity, circuit delay, power supply noise, logic noise margin values,~~ threshold voltage value[[,]] or clock frequency value.

14. (Previously Presented) The method according to claim 17, wherein the pre-set level of performance relates to at least one of power consumption or speed of the integrated circuit.

15. (Previously Presented) The method according to claim 17, wherein the integrated

circuit is designed based on utility values different from nominal values.

16. (Currently Amended) An integrated circuit, comprising:

a plurality of computation islands operating at one or more utility values, at least one utility value of a first computation island of the plurality of computation islands being different from a corresponding at least one utility value of a second computation island of the plurality of computation islands; [[and]]

a global monitor configured to monitor at least one working parameter related to a working condition of the integrated circuit; and

at least one interface island for interfacing at least two of the plurality of computation islands,

wherein each of the first and second computation islands comprises a local controller for independently tuning the corresponding at least one utility value based on the monitored at least one working parameter, the local controller communicating with a global controller to obtain a pre-set level of performance of the integrated circuit.

17. (Currently Amended) A method for real-time tuning of at least one utility value of an integrated circuit, comprising a plurality of computation islands operating at one or more utility values, each of the computation islands comprising a local controller for independently tuning the at least one utility value for the computation island, the method comprising:

monitoring at least one working parameter related to a working condition of the integrated circuit;

independently tuning the at least one utility value for at least one computation island of the plurality of computation islands using the corresponding local controller, based on the monitored at least one working parameter; and

controlling each local controller of each computation island using a global controller to obtain a pre-set level of performance of the integrated circuit,

wherein the at least one working parameter comprises at least one of circuit activity,

circuit delay, power supply noise, or logic noise margin values.

18. (Previously Presented) An integrated circuit, comprising:

a first computation island having a first value of a utility value, the first computation island comprising a first local controller and a first actuator;

a second computation island having a second value of the utility value, the second computation island comprising a second local controller and a second actuator, the second computation island being isolated from the first computation island;

an interface island for interfacing the first and second computation islands;

a global monitor configured to monitor a working parameter related to a working condition of the integrated circuit; and

a global controller configured to determine a range of the utility value for each of the first computation island and the second computation island based on the monitored working parameter,

wherein each of the first and second local controllers obtains a pre-set level of performance of the integrated circuit from the global controller and independently tunes the utility value within the range of the utility value based on the monitored at least one working parameter.